UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,454	07/17/2002	Kuang-Kai Kuo	8327-US-PA	5796

31561 7590 12/20/2005		EXAMINER
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE		VITAL, PIERRE M
7 FLOOR-1, NO. 100		
ROOSEVELT ROAD, SECTION 2	ART UNIT	PAPER NUMBER
TAIPEI, 100	2188	
TAIWAN		

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	**Applicant(s)**
Office Action Summary	10/064,454	KUO ET AL.
	Examiner	**Art Unit**
	Pierre M. Vital	2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _11 October 2005_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-6 and 8-11_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-6 and 8-11_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _05 February 2004_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

1.   This Office Action is in response to applicant's communication filed September 15, 2004 in response to PTO Office Action mailed October 11, 2005. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2.   In response to the last Office Action, no claims have been amended. No claims have been canceled. No claims have been added. As a result, claims 1-6 and 8-11 remain pending in this application.

Response to Arguments

3.   Applicant's arguments filed October 11, 2005 have been fully considered but they are not persuasive. As to the Remarks, applicant asserted that:

(a)   The prior art of record does not teach "wherein said first section read address and said second section read address are compared respectively before they are combined" as recited in independent claims 1 and 8.

Examiner agrees with applicant that Pollack does not teach combining strings. However, Examiner would like to point out that Pollak discloses that multiple characters (i.e., combination of characters) form a string. Pollack further teaches that the

characters (i.e., sections of strings) in the strings are compared successively (column 1,

lines 62-67). Thus, by successively comparing the characters, Pollak clearly teaches

that these characters (i.e., sections of strings) are compared to detect mismatches

before they are combined into strings (i.e., before the data are totally received). Also

note that the comparison is quickly performed while searching file system directories

(column 1, lines 47-49).

As such, it can be clearly seen that Pollack discloses the combination of

characters (i.e., sections of string) before these characters are combined into strings.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 1, 5-6, 8 and 10-1 1 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Becker (US 5,379,379) in view of Mills (US 5,497,355) and Pollak

(US 6,618,724).

As in claim 1, Becker describes a memory control system coupled to a system

bus (Figs. 1 and 5a, elements 12 and 224 column 3, lines 1 1-16 and 30-33) and having

a clock line (Figs. 3a-3c, element labeled (KCLK'" column 6, lines 28-38), where the

memory control system comprises:

a memory write command queue for holding a plurality of memory write

commands, wherein each said memory write command has an address (Fig. 5a,

elements 90 and 92; column 8, lines 53-57);

wherein the memory control system receives a read address of a read command

(i.e. a memory read operation) according to a clock signal (Fig. 1; column 4, lines 31-36;

Figs. 3b-3c; column 6, lines 43-62; column 8, lines 1-17);

a memory request organizer function wherein the read address is compared with

the write address of each memory write command in the memory write command

queue, and if the comparison indicates the presence of identical bits, the execution of

the memory read command is delayed until the matching memory write commands in

the memory write command queue execute (column 9, lines 1-9; column 12, lines 19-

35); and wherein if the comparison indicates a difference, execution of the memory read

command is permitted (Column 12, lines 63-66).

Becker does not teach that the read address is received sequentially by a bus

interface unit as a first and second section, and that the first and second sections are

output concurrently, as required by claim 1.

Mills teaches an address demultiplexer coupled to a memory' request bus (i.e. a

bus interface unit) where an address is received sequentially as a row address (i.e. first

section) and column address (i.e. second section), and the row and column addresses

are output concurrently (Fig. 5, column 13, lines 3-13). Mills teaches that this arrangement allows synchronous address latching circuitry to work with multiplexed addresses such as those occurring in dynamic random access memories (Column 12, lines 57-60).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the address demultiplexing arrangement taught by Mills, in the system of Becker, in order to allow synchronous address latching circuitry to work with multiplexed addresses as taught by Mills.

The combination of Becker and Mills does not teach a two-step comparison algorithm where the first section read address is first compared, and the second section read address is compared if the first section read address indicates a match, wherein said first section read address and said second section read address are compared respectively before they are combined as required by claim 1.

Pollak teaches a string comparison algorithm where characters comprising identical bit portions of two strings are compared such that if the first characters match (i.e. first section), the second characters (i.e. second section) are subsequently compared, but if the first characters do not match, the comparison is terminated and execution of a controlling process continues (Fig. 2, column 4, lines 18-39). It is further noted that Pollak teaches that characters (i.e., sections) in the strings are successively

compared (i.e., compared before they are combined) (column 1, lines 62-67). It may be understood from the teaching of Pollak that by stopping the comparison after the first mismatch is found, the time required to compare the strings is less than if the entire strings were compared (column 1, line 66 to column 2, line 4).

Regarding claim 1, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to compare the read address as a series of subsequent comparisons on a first and second section of the read address and the first and second section read addresses before they are combined as in the comparison algorithm taught by Pollak, in the system made obvious by the combined teachings of Becker and Mills, due to the similarity in the nature of the problem to be solved, namely the comparison of unitary collections of bits, and in order to reduce the time required to make the comparison as taught by Pollak.

Regarding claims 5-6, although the combination of Becker, Mills and Pollak does not teach that when comparing the first and second sections of the read and write addresses, the first section of the address includes bits 12 to 31, and that the second section of the address includes bits 6 to 11, such limitations are merely a matter of design choice and would have been obvious in the system of Becker, Mills and Pollak. Becker, Mills and Pollak teach a comparison made between the first sections of a read and write address, and a comparison made between the second sections of a read and write address. The limitations in claims 5-6 of the instant application do not define a

patentably distinct invention over Becker, Mills and Pollak since both are directed

toward comparing addresses that are divided into two distinct portions. The particular

assignment of bit ranges to these portions is inconsequential for the invention as a

whole and presents no new or unexpected result. Therefore, to assign bits 12 to 31 as

the first section of the address, and to assign bits 6 to 11 as the second section of the

address would have been an obvious design choice to one of ordinary skill in the art at

the time of invention by applicant.

Method claim 8 is rejected using the same rationale as for the rejection of claim 1

above.

As in claim 10, Becker teaches that a memory read command may be output

directly via a fast path, and that a memory read command may alternatively be

transferred to a memory read command queue (Fig. 5a, elements 94, 152 and "FAST'"

column 15, line 50 to column 16, line

As in claim 11, Becker teaches a flag for permitting execution of the memory

read command after the memory read command is received and when the comparison

between the read and write addresses indicates a difference (Fig. 5a, "RAMTCH"

column 11, line 67 to column 12, line 35). It is noted that Becker teaches de-asserting

the flag when a comparison indicates a difference, however, the use of positive and

negative meanings for signals are well known in the art, and one of ordinary skill in the

art would recognize that the de-assertion of a signal is equivalent to the assertion of its

opposite meaning. Therefore, it would have been obvious to raise a flag when the

comparison indicates a difference in the system of Becker, Mills and Pollak.

6.   Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Becker (US 5,379,379), Mills (US 5,497,355) and Pollak (US 6,618,724) as applied to

claim 1 above, and further in view of Mann (US 5,954,813).

Becker, Mills and Pollak are relied upon for the teachings relative to claim 1 as

above.

The combination of Becker, Mills and Pollak does not teach the following

limitations required by claims 2-3:

a first and second compare unit coupled to the bus interface unit for receiving the

first and second section read addresses, respectively, and comparing the first and

second section read addresses to the identical bit portions of each write address of the

memory write commands inside the memory write command queue, and outputting a

first and second comparison signal; and

a grant decision unit coupled to the first and second comparison units, wherein a

grant execution signal is set if either compare unit indicates a difference, otherwise the

grant execution signal is set only after the memory write command with identical

address bits executes.

Referring to the rationale for the rejection of claim 1, it is noted that Becker, Mills and Pollak teach the comparison of a read address against the write addresses in a memory write command queue, and granting execution of the read command if there is no match, and delaying execution of the read command until the matching write command executes if there is a match.

However, Becker, Mills and Pollak do not teach the specific configuration of the comparison function enumerated above, particularly the use of two compare units and a grant decision unit.

Mann teaches the comparison of an address divided into a first and second section against a stored address using two comparators (i.e. compare units), where a control unit (i.e. grant decision unit) receives the results of the comparison from each comparator and outputs a signal (i.e. grant execution signal) to allow the continued execution of a process if the addresses do not match, and halt execution of a process if the addresses match (Fig. 3; column 3, lines 47-55; column 6, lines 11-52).

Regarding claims 2-3, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the address comparison configuration taught by Mann to execute the address comparison function in the system made obvious by the combination of Becker, Mills and Pollak, as suggested by the similarity in

the nature of the problem to be solved which would have been recognized by one of

ordinary skill in the art at the time of the invention.

Regarding claim 3, the rationale derived from Becker in the rejection of claim 10

above is incorporated herein for the teaching that a memory read command may be

output directly via a fast path, and that a memory read command may alternatively be

transferred to a memory read command queue.

7.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Becker

(US 5,379,379), Mills (US 5,497,355) and Pollak (US 6,618,724) as applied to claim 1

above, and further in view of applicant's admitted prior art (APA).

Becker, Mills and Pollak are relied upon for the teachings relative to claim 1 as

above.

The combination of Becker, Mills and Pollak does not teach that transfer of the

first section read address requires two bit times, where a rising edge and a falling edge

of the clock are both defined as a bit time, as required by claim 4.

APA describes a system bus defined by AMD Corporation where each rising and

falling edge of the clock signal is defined to be a single bit time unit and the first section

read address is transmitted in two bit time units (Page 4, paragraph 9).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to define each rising and falling edge of the clock signal to be a single bit time unit, and to require two bit time units to transfer the first section read address, in the system made obvious by the combination of Becker, Mills and Pollak, as suggested by the applicant's own admitted prior art.

8.   Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (US 5,379,379), Mills (US 5,497,355) and Pollak (US 6,618,724) ms applied to claim 8 above, and further in view of applicant's admitted prior art (APA).

Becker, Mills and Pollak are relied upon for the teachings relative to claim 8 as above.

The combination of Becker, Mills and Pollak does not teach that transfer of the first section read address requires two bit times, where a rising edge and a falling edge of the clock are both defined as a bit time, as required by claim 9.

The rationale set forth in the rejection of claim 4 is applied herein for the rejection of claim 9.

Conclusion

9.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

10.   The examiner requests, in response to this Office action, support be shown for

language added to any original claims on amendment and any new claims. That is,

indicate support for newly added claim language by specifically pointing to page(s) and

line no(s) in the specification and/or drawing figure(s). This will assist the examiner in

prosecuting the application.

11.   When responding to this office action, Applicant is advised to clearly point out the

patentable novelty which he or she thinks the claims present, in view of the state of the

art disclosed by the references cited or the objections made. He or she must also show

how the amendments avoid such references or objections See 37 CFR 1.111(c).

12.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Pierre M. Vital whose telephone number is (571) 272-

4215. The examiner can normally be reached on 8:30 am - 6:00 pm, alternate Fridays

off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

December 12, 2005

PIERRE VITAL
PRIMARY EXAMINER